LISTING OF CLAIMS

1. (Currently Amended) A stream routing unit configured to route ~~for routing~~ each of a plurality of input packet streams to any of a plurality of destinations, the stream routing unit comprising:

a plurality of input ports configured to receive ~~for receiving~~ respective input streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

a store configured to hold ~~storage means for holding~~ packets of the input packet streams at ~~arbitrarily~~ addressable locations each identifiable by an address, said store being shared by all of said input ports and said output ports;

an assignment data structure configured to identify ~~identifying~~ for each source of the input packet stream at least one destination to which each input packet stream is to be routed;

a packet allocation table comprising an array including a plurality of slots configured to hold ~~holding~~ for each ~~new~~ incoming packet a source identifier that identifies ~~identifying~~ the source of the incoming packet and the ~~arbitrary~~ address in the store ~~storage means~~ where the incoming packet is held, the packet allocation table further including a plurality of destination pointers, each destination pointer associated with one of the output ports, each destination pointer being assignable to any slot so as to identify the output ports associated with the intended destinations of a held packet, the assigning of each destination pointer to a slot being derived using the assignment data structure; and

a processor configured to control ~~processing means for controlling~~ the removal of packets from the store and the sending of the removed packets out through ~~storage means to~~ the plurality of output ports using the assigned destination pointers, wherein an order of packet removal from the store for sending out through the output ports depends on whether the output ports through which the removed packets are to be sent based on the assigned destination pointers are free to send out packets.

2. (Original) The stream routing unit according to claim 1, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

3. (Previously Presented) The stream routing unit according to claim 1, wherein the assignment data structure is a data matrix.

4. (Canceled).

5. (Previously Presented) The stream routing unit according to claim 1, wherein the packet allocation table is associated with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

6. (Canceled).

7. (Original) The stream routing unit according to claim 1, wherein the packets of a said input stream are of a common length.

8. (Currently Amended) A data communication system configured to route ~~for routing~~ incoming packets to at least one destination, the system comprising:

a plurality of packet stream sources each generating a packet stream;

a stream routing unit comprising:

a plurality of input ports configured to receive ~~for receiving~~ respective input packet streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

a store configured to hold ~~storage means for holding~~ packets of the input packet streams at ~~arbitrarily~~ addressable locations each identifiable by an address, said store being shared by all of said input ports and output ports;

an assignment data structure configured to identify ~~identifying~~ for each source of the input packet stream at least one destination to which each input packet stream is to be routed;

a packet allocation table comprising an array including a plurality of slots configured to hold ~~holding~~ for each ~~new~~ incoming packet a source identifier configured to identify ~~identifying~~ the source of the incoming packet and the ~~arbitrary~~ address in the store ~~storage means~~ where the incoming packet is held, the packet allocation table further including a plurality of destination pointers, each destination pointer associated with one of the output ports, each destination pointer being assignable to any slot so as to identify the output ports associated with the intended destinations of a held packet, the assigning of each destination pointer to a slot being derived using the assignment data structure; and

a processor configured to control ~~processing means for controlling~~ the removal of packets from the store and the sending of the removed packets out through ~~storage means to~~ the plurality of output ports using the assigned destination pointers, wherein an order of packet removal from the store for sending out through the output ports depends on whether the output ports through which the removed packets are to be sent based on the assigned destination pointers are free to send out packets; and

a plurality of destinations for receiving packets of the packet streams generated by the sources.

9. (Original) The data communication system according to claim 8, wherein at least one of the destinations comprises a programmable transport interface.

10. (Original) The data communication system according to claim 8, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

11. (Currently Amended) A method of routing packet streams from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams at a plurality of input ports each having an input port identifier;

providing an assignment data structure identifying for each input port identifier ~~source of the input packet stream~~ at least one intended output port ~~destination~~ to which the ~~each input~~ packet stream received at the input port is to be routed ~~using an assignment data structure~~;

holding each packet of the packet stream in a store ~~storage means~~ at an ~~arbitrarily~~ addressable location identifiable by an address in that store ~~storage means~~;

providing ~~holding for each new incoming packet~~ a packet allocation table comprising an array including a plurality of slots, each slot storing the input port ~~which stores a source~~ identifier of ~~identifying~~ the input port which received a ~~source of the~~ packet from one of the packet streams and the ~~arbitrary~~ address in the store ~~storage means~~ where the received packet is held ~~; holding information in an assignment data structure identifying for each source at least one intended destination of the packet~~;

providing a plurality of destination pointers, each destination pointer associated with an output port ~~for one of the destinations~~, each destination pointer being assignable to any slot of the packet allocation table ~~so as to identify the output ports associated with the intended destinations of a held packet~~;

using said assignment data structure ~~information~~ identifying the intended output port for each input port identifier ~~destination from the packet source~~ to assign each destination pointer to a slot of the packet allocation table based on the output port associated with the destination pointer and the input port identifier that is stored in the slot and identified with that output port by the assignment data structure;

retrieving the packet from the store ~~memory means~~ at the ~~arbitrary~~ address contained in the slot to which each destination pointer is assigned; and

routing the addressed packet from the store ~~storage means~~ to the or each output port associated with the assigned ~~respective~~ destination pointer(s).

12. (Original) The method according to claim 11, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the output ports.

13. (Canceled).

14. (Currently Amended) The method according to claim 11 further comprising:

associating each slot with a write pointer which is configured to point to the next available slot in the array for storing the input port ~~source~~ identifier and address of the received ~~next incoming~~ packet.

15. (Currently Amended) A device for delivering incoming packets to at least one destination, the device comprising:

a plurality of input ports, each input port having an input port identifier;

a plurality of output ports;

an addressable memory configured to store ~~which stores~~ incoming packets at a plurality of address locations in the memory;

a ~~source to destination~~ matrix configured to map ~~for mapping~~ at least one input port identifier ~~source~~ to at least one output port ~~destination~~;

a packet allocation table including a plurality of slots, each slot configured to associate an input port identifier ~~associating a source~~ for the input port at which a particular packet is received with the address location in the addressable memory where the particular packet is stored;

a plurality of destination pointers associated with the packet allocation table, each destination pointer having an associated output port ~~destination~~, and each destination pointer being assignable to any slot in the packet allocation table; and

an algorithm configured to control ~~for controlling~~ removal of the incoming packets from the [[a]] memory to at least one output port ~~destination~~, the algorithm assigning each destination pointer to a slot in the packet allocation table based on the ~~source~~ output port associated with the destination pointer and the input port identifier within the slot of the packet allocation table and mapped to the output port by the ~~destination information within the source to destination~~ matrix, wherein the packet at the address location within the slot of the packet allocation table assigned to the destination pointer is retrieved from the addressable memory and delivered to the output port associated with that destination pointer ~~at least one destination~~.

Claims 16-31. (Canceled).

32. (Currently Amended) The stream routing unit according to claim 1 ~~6~~, wherein the destination pointers are assigned by an algorithm.

33. (Currently Amended) The stream routing unit according to claim 32, wherein after the assignment of destination pointers is completed, the algorithm controls the store ~~storage means~~ to output a packet according to the assigned ~~status of the~~ destination pointers.

34. (Previously Presented) The stream routing unit according to claim 1, wherein held packets are output in the order in which they are received.

35. (Currently Amended) The stream routing unit according to claim 1, wherein ~~further comprising means for outputting~~ the held packet is output only when all of the output ports associated with the intended destinations of the held packet are free.

36. (Currently Amended) A stream routing unit, comprising:

a plurality of input ports, each input port configured to receive ~~receiving~~ an input packet stream;

a plurality of output ports, each output port configured to output ~~outputting~~ an output packet stream;

a memory including a plurality of addressable memory locations;

a ~~source-to-destination~~ matrix configured to map ~~mapping~~ each input port receiving ~~source of~~ the input packet streams ~~coupled to the input ports~~ to one or more output ports ~~destinations,~~ for receiving the packets within those input packet streams ~~, which are coupled to receive the output packet streams from the output ports~~;

an insertion circuit configured to insert into a header of each packet of the received input packet stream an input port identifier for the input port which received the input packet stream;

a processor configured to store ~~for storing~~ packets of the input packet streams in the memory and configured to retrieve ~~for retrieving~~ stored packets from the memory to form the output packet streams;

the processor configured to fill ~~filling~~ a packet allocation table which includes a plurality of slot locations, each slot location storing the input port identifier from the packet header ~~a source identifier~~ which identifies the input port that ~~a source of the~~ received the input packet stream to which a given packet belongs linked in the slot of the packet allocation table to an address in the memory for the addressable memory location where that given packet has been stored by the processor;

a destination pointer, associated with each one of the output ports, implemented by the processor and configured to point ~~for pointing~~ to a slot location in the packet allocation table from which the address of the given packet is retrieved, the destination pointer pointing to the slot location when the input port ~~source~~ identifier in the slot matches the input port identifier ~~is associated with a source that is~~ mapped through the ~~source-to-destination~~ matrix to ~~a destination coupled to~~ an output port ~~and that output port is~~ associated with that destination pointer;

the processor further configured to retrieve ~~retrieving~~ the given packet from the memory at the address provided in the slot location pointed at by the destination pointer, and send ~~sending~~ the retrieved given packet to each output port associated with that destination pointer for inclusion in the output packet stream of the output port.

37. (Currently Amended) The stream routing unit of claim 36 further comprising a write pointer implemented by the processor and configured to point ~~processing means for pointing~~ to an open slot location in the packet allocation table to which the source identifier and address of the given packet are written.

38. (Previously Presented) The stream routing unit of claim 36, wherein a bit rate of the input packet streams is lower than a bit rate of the output packet streams.

39. (New) A method of routing packet streams from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams at a plurality of input ports;

storing each packet of the packet stream at an addressable location identifiable by an address;

providing an assignment data structure identifying for each source of the input packet stream at least one destination to which the packet stream received at the input port is to be routed;

providing a packet allocation table comprising an array including a plurality of slots, each slot storing a source identifier of identifying the source of the packet from one of the packet streams and the address of the location where the received packet is stored;

providing a plurality of destination pointers, each destination pointer associated with an output port for one of the destinations, each destination pointer being assignable to any slot of the packet allocation table so as to identify the output ports associated with the intended destinations of a stored packet;

using said assignment data structure identifying the intended destination from the packet source to assign each destination pointer to a slot of the packet allocation table;

removing stored packets from the address contained in the slot to which each destination pointer is assigned, wherein an order of packet removal for sending out through the output ports depends on whether the output ports through which the removed packets are to be sent based on the assigned destination pointers are free to send out packets; and

routing the addressed packet to the or each output port associated with the assigned destination pointer(s).

40. (New) A stream routing unit, comprising:

a plurality of input ports, each input port configured to receive an input packet stream;

a plurality of output ports, each output port configured to output an output packet stream;

an insertion circuit coupled to the input ports and adapted to receive the input packet streams and insert into a header of each packet in the received input packet stream an input port identifier of the input port which received that input packet stream;

a matrix configured to map an assignment of which output ports of the stream routing unit are to output the packet streams received at each input port;

a memory including a plurality of addressable memory locations, the memory adapted to store packets from the received input packet streams at the addressable memory locations;

a packet allocation table including a plurality of slot locations, each slot location storing a) the input port identifier from the packet header which identifies the input port that received the input packet stream to which a given packet belongs and b) an address in the memory for the addressable memory location where that given packet has been stored;

a destination pointer, associated with each one of the output ports, each destination pointer being assigned to point to one of the plurality of slot location when the input port identifier in the slot matches the input port identifier mapped through the matrix to an output port associated with that destination pointer;

a processor configured to retrieve the given packet from the memory at the address provided in the slot location pointed at by each destination pointer, and send the retrieved given packet to the output port associated with that destination pointer for inclusion in the output packet stream at the output port.